Abstract of the Disclosure

A high voltage insulated gate field-effect transistor includes an insulated gate field-effect device structure having a source and a drain, the drain being formed with an extended well region having one or more buried layers of opposite conduction type sandwiched therein. The one or more buried layers create an associated plurality of parallel JFET conduction channels in the extended portion of the well region. The parallel JFET conduction channels provide the HVFET with a low on-state resistance.